TABLE OF CONTENTS

TABLE OF CONTENTS ......................................................................................................... 1
LIST OF FIGURES ................................................................................................................ 1
LIST OF TABLES .................................................................................................................. 1
1. DESCRIPTION ................................................................................................................ 2
   1.1. FUNCTIONAL DESCRIPTION ......................................................................... 2
2. SPECIFICATIONS ........................................................................................................... 5
   2.1. EXTERNAL COMPONENTS ............................................................................ 5
   2.2. INTERNAL COMPONENTS ........................................................................... 5
   2.3. POWER REQUIREMENTS ............................................................................ 5
   2.4. CHARACTERISTICS OF THE SIGNALS ......................................................... 6
   2.5. TIMING DIAGRAM ........................................................................................... 7
3. OPERATING MODES ..................................................................................................... 10
   3.1. GENERAL INFORMATION .............................................................................. 10
   3.2. POWER-UP CONFIGURATION ....................................................................... 11
   3.3. INTERRUPT PROGRAMMING ........................................................................ 11
   3.4. V1/V2 OUTPUT SETTING (FOR THE A544 BOARDS) ....................................... 11
   3.5. CIRCULAR BUFFER LENGTH PROGRAMMING ........................................... 11
   3.6. CONFIGURATION REGISTER PROGRAMMING ........................................... 12
   3.7. DATA ACQUISITION ....................................................................................... 12
   3.8. CIRCULAR BUFFER TEST .............................................................................. 12
4. VME INTERFACE .......................................................................................................... 13
   4.1. ADDRESSING CAPABILITY ............................................................................ 13
   4.2. INTERRUPT LEVEL/VECTOR REGISTER ...................................................... 14
   4.3. STATUS REGISTER ......................................................................................... 15
   4.4. EVENT NUMBER REGISTER .......................................................................... 16
   4.5. V1/V2 OUTPUT SET REGISTERS .................................................................... 16
   4.6. RESET REGISTER .......................................................................................... 17
   4.7. CONFIGURATION REGISTER ........................................................................ 18
   4.8. ENABLE/DISABLE ACQUISITION ................................................................... 18
   4.9. FIFO HIGH READOUT .................................................................................... 18
   4.10. FIFO LOW READOUT .................................................................................... 18
   4.11. FIFO WRITING REGISTER ........................................................................... 18
   4.12. LOAD REGISTER ........................................................................................... 19
   4.13. CLOCK REGISTER ....................................................................................... 19
   4.14. TRIGGER REGISTER ..................................................................................... 19

LIST OF FIGURES

Fig. 1.1: V533 Block Diagram. ................................................................................................ 4
Fig. 2.1: V533 Timing Diagram ............................................................................................... 7
Fig. 2.2: V533 Front Panel ....................................................................................................... 8
Fig. 2.3: V533 Components Locations ...................................................................................... 9
Fig. 4.1: Mod. V533 Base Address Setting. ............................................................................. 14
Fig. 4.2: INTERRUPT Level/Vector Register ........................................................................ 15
Fig. 4.3: Status Register ....................................................................................................... 15
Fig. 4.4: Event Number Register ........................................................................................... 16
Fig. 4.5: V1/V2 Output Set Registers .................................................................................... 16
Fig. 4.6: Configuration Register. ........................................................................................... 18

LIST OF TABLES

Table 4.1: Address Map for the Mod. V533 ........................................................................ 13
1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The CAEN Model V533 is a 32 CHANNEL PIPELINE UNIT housed in a 1-unit wide VME module, provided with 32 TTL differential input channels (a functional block diagram is shown in Fig. 1.1). The purpose of this module is to store in a pipeline buffer a certain number of words that can be retrieved upon occurrence of a trigger signal (that is delayed with respect to the cause of the trigger itself) without stopping the acquisition.

The module houses a pipeline FIFO (256x32 bits) that implements a circular buffer. The buffer length can be programmed via VME up to 255 words. At each pulse of the external CLOCK frequency (65 MHz maximum) the new input data are stored in the FIFO; when the programmed buffer length is reached, each oldest datum is lost with the storage of each new input datum.

In NORMAL MODE, at the arrival of an external TRIGGER, the oldest data contained in the pipeline memory are transferred to a multi-event buffer 256x32 bit deep. The length of the block of 32-bit words to be transferred can be programmed via VME and ranges from 3 to 15.

In TRANSPARENT MODE, at the arrival of an external TRIGGER and for all the duration of the TRIGGER signal itself, the oldest data will be transferred to the multi-event buffer without any block length limitation.

The TRIGGER signal also increments an Event Counter whose content is stored in a further FIFO memory 256x8 bit deep, that allows to associate an event number to the block of words transferred to the Multi-event buffer.

The 32 input signals, together with an external input "OR" via front panel LEMO 00 connector, are sent also to an OR logic that implements the following functions:

- a global OR between the 32 inputs and the front panel OR input;
- the 16 ORs of the inputs in groups of 2;
- the 8 ORs of the inputs in groups of 4;
- the 4 ORs of the inputs in groups of 8;
- the 2 ORs of the inputs in groups of 16.

The global OR is available on a LEMO 00 output connector, and allows to obtain a global OR of many V533 units. Each of the other 4 OR functions is selectable via VME and is available on the front panel DIGOR OUT connector.

The module houses a VME INTERRUPTER that generates a VME interrupt (if enabled) in these conditions:

- when the Trigger input becomes TRUE;
- when the Multi-event buffer is Full.

The Pipeline Memory operation is stopped when the Multi-event buffer is Full (Module BUSY) or upon occurrence of an external BUSY. These conditions are signalled via an open-collector signal available on the Front Panel (BUSY); this allows to obtain a wired-OR Global Busy of many V533 units. The Busy input/output is provided with two bridged connectors for daisy chaining.
Upon request it is possible to have a module housing a Multi-event buffer with length up to 4096 words, with 50 MHz operating frequency.

A front panel LED (DTACK) lights up each time the module generates the VME signal DTACK. The data contained in the event buffer are accessible via VME and can be read also in Block Transfer mode (D32 only).

The Model V533 uses the P1 and P2 connectors of VME and the auxiliary connector for the CERN V430 VMEbus crate (Jaux Dataway).

The module works in A24 mode; the recognized Address Modifier codes are:

\[
\begin{align*}
AM &= \%3D \quad \text{standard supervisor data access;} \\
AM &= \%39 \quad \text{standard user data access;} \\
AM &= \%0D \quad \text{extended supervisor data access;} \\
AM &= \%09 \quad \text{extended user data access.}
\end{align*}
\]

The module’s Base Address is fixed by 2 internal rotary switches housed on a piggy-back board plugged into the main printed circuit board. The Base Address can be selected in the range:

\[
%00\ 0000 \leftrightarrow %FF\ 0000 \quad \text{A24 mode.}
\]

The data transfer occurs in D16/D32 mode.

The Model V533 can be used for the parallel readout of the data coming from a CAEN A544 board (for Resistive Plate Counters front end). To this purpose, it provides also two programmable analog voltages ($\pm 5$ V in steps of 40 mV) to control the Threshold and Width lines of the A544 board.
Fig. 1.1: V533 Block Diagram
2. SPECIFICATIONS

2.1. EXTERNAL COMPONENTS

CONNECTORS

- No. 1, "IN 0..16", input connector, Header 3M 3431-5202 type, 17+17 pins. Connector for the INPUT differential TTL signals.

- No. 1, "IN 17..31, GND, V1, V2", input/output connector, Header 3M 3431-5202 type, 17+17 pins. Connector for the INPUT differential TTL signals, the GROUND reference and the V1, V2 output voltage levels.

- No. 1, "OR IN", input connector, LEMO 00 type. Connector for the OR IN signal.

- No. 1, "OR OUT", output connector, LEMO 00 type. Connector for the OR OUT signal.

- No. 1, "TRIG", input connector, LEMO 00 type. Connector for the TRIGGER signal.

- No. 2, "BUSY", input/output bridged connectors, LEMO 00 type. Connectors for the BUSY signal.

- No. 2, "CLK", input bridged connectors, LEMO 00 type. Connectors for the external CLOCK signal.

- No. 1, "DIGOR OUT", output connector, Condo Header 3M 3408-D202 type, 2*(8+8) pins. Connector for the "Digital OR" output signal.

DISPLAYS

- No. 1, "DTACK", green LED, VME Selected; it lights up during a VME access.

2.2. INTERNAL COMPONENTS

SWITCHES

- No. 2, rotary switches for the module VME BASE address selection.

2.3. POWER REQUIREMENTS

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>+12 V</td>
<td>160 mA</td>
</tr>
<tr>
<td>-12 V</td>
<td>160 mA</td>
</tr>
<tr>
<td>+5 V</td>
<td>2 A</td>
</tr>
<tr>
<td>-5 V</td>
<td>160 mA</td>
</tr>
</tbody>
</table>
2.4. CHARACTERISTICS OF THE SIGNALS

INPUTS:

- IN 0..31: Differential TTL level, 110 Ω impedance;
  Minimum width: 25 ns.
  Setup Time (ref.'d to CLK): min. 0 ns;
  Hold Time (ref.'d to CLK): min. 15 ns.

- OR IN: Std. NIM Level, 50 Ω impedance;
  Minimum width: 50 ns.

- TRIG: Std. NIM level, 50 Ω impedance;
  Minimum width: 20 ns;
  Maximum width: < 3xCLK period (NORMAL MODE).

- CLOCK: Std. NIM level, 50 Ω impedance;
  Maximum frequency: 65 MHz;
  Duty cycle: 50%.

OUTPUTS:

- OR OUT: Std. NIM level on 50 Ω impedance.

- DIGOR OUT: Differential ECL level on 110 Ω impedance.

- V1, V2: Programmable voltage levels (±5 V in steps of 40 mV).

- BUSY: TTL level, high impedance.
2.5. TIMING DIAGRAM

The diagrams here below correspond to 2 examples:

a) in NORMAL mode the Configuration Register setting (bits 0::3) is set to Block Length=7.
b) in TRANSPARENT mode a Trigger signal of approximate duration of 8 CLock cycles is shown.

NORMAL MODE

N. of Words to be transferred: 7 (Control Register setting)

TRANSPARENT MODE

N. of transferred Words: 8 (depends on the Trigger signal duration)
Fig. 2.2: Mod. V533 Front Panel
Component side of the board

Fig. 2.3: Mod. V533 Components Locations
3. OPERATING MODES

3.1. GENERAL INFORMATION

The V533 module houses a pipeline FIFO (256x32 bits) that implements a circular buffer. The buffer length can be programmed via VME up to 255 words. At each pulse of the external CLOCK frequency (65 MHz maximum) the new input data are stored in the FIFO; when the programmed buffer length is reached, each oldest datum is lost with the storage of each new input datum.

In NORMAL MODE, at the arrival time of an external TRIGGER (plus 2 or 3 CLK cycles for resynchronization, see Fig. 2.1), the oldest data contained in the pipeline memory are transferred to a multi-event buffer 256x32 bit deep. The length of the block of 32-bit words to be transferred can be programmed via VME and ranges from 3 to 15.

In TRANSPARENT MODE, at the arrival time of an external TRIGGER (plus 2 or 3 CLK cycles for resynchronization, see Fig. 2.1) and for all the duration of the TRIGGER signal itself, the oldest data will be transferred to the multi-event buffer without any block length limitation.

The TRIGGER signal also increments an Event Counter whose content is stored in a further FIFO memory 256x8 bit deep, that allows to associate an event number to the block of words transferred to the Multi-event buffer. The Event Number readout must be performed together with the Data readout, in order to maintain the correct association between the two informations.

The 32 input signals, together with an external input "OR" via front panel LEMO 00 connector, are sent also to an OR logic that implements some logic functions (see § 4.7).

The Pipeline Memory operation is stopped when the Multi-event buffer is Full (Module BUSY) or upon occurrence of an external BUSY. These conditions are signalled via an open-collector signal available on the Front Panel (BUSY); this allows to obtain a wired-or Global Busy of many V533 units. The Busy input/output is provided with two bridged connectors for daisy chaining.

The purpose of this module is to store in a pipeline buffer a certain number of words that can be retrieved upon occurrence of a trigger signal (that is delayed with respect to the cause of the trigger itself) without stopping the acquisition: if, e. g., the User wants to read 7 words of the pipeline in an interval that includes the trigger, and the delay of the trigger signal respect to the cause of the trigger itself is equivalent to n CLOCK cycles, He/She can program a buffer length of n+3 and a number of words to be transferred of 7. Upon arrival of the Trigger signal, 7 words will be transferred to the Multi-event buffer, the 4th being the word corresponding to the time of the trigger cause occurrence.
3.2. POWER-UP CONFIGURATION

After a setting of the module Address via rotary switches (see § 4.1) the module can be inserted in a VME crate and powered-on.

At Power-On the module is in the following condition:
- The bit PAF of the STATUS Register (§ 4.3) is set to 1, the other bits of this Register are set to 0;
- The INTERRUPT Register is cleared;
- The Event Number, V1/V2 Set, Configuration and ENABLE/DISABLE Acquisition Registers' content is not defined.

3.3. INTERRUPT PROGRAMMING

The INTERRUPT generation occurs upon receipt of a trigger signal or upon filling-up of the Buffer Memory (PAF bit set to 0). The removal of the INTERRUPT condition occurs in the former case inside the INTERRUPT cycle itself, in the latter case by reading out the Multi-event Buffer until the PAF bit becomes 1.

The INTERRUPT Level and STATUS/ID can be programmed by writing into the INTERRUPT Register, see § 4.2.

3.4. V1/V2 OUTPUT SETTING (FOR THE A544 BOARDS)

The V533 module can be used in conjunction with the A544 model to perform the readout of an RPC (Resistive Plate Counters) based System. In order to program via VME the Threshold and the Gate Width of the A544 model, the User can set a value in two different Registers, V1 Output Set and V2 Output Set, which corresponds to an output voltage between -5 V and +5 V on the two pins V1 and V2 of the output connector (see § 4.5).

3.5. CIRCULAR BUFFER LENGTH PROGRAMMING

In order to program the Circular Buffer length, the User must perform the following operations in the correct order:

- Disable the Acquisition (§ 4.8);
- Set to 0 the LOAD line (§ 4.12);
- RESET the module (§ 4.6);
- Write a value of 0 in the FIFO Writing Register (§ 4.11);
- Perform one time an access to the CLOCK Register (§ 4.13);
- Write a value of (255 - DESIRED LENGTH) in the FIFO Writing Register (§ 4.11);
- Perform an access to the CLOCK Register (§ 4.13);
- Write a value of 0 in the FIFO Writing Register (§ 4.11);
- Perform an access to the CLOCK Register (§ 4.13);
- Set to 1 the LOAD line (§ 4.12);
- Enable the Acquisition if desired (§ 4.8).

N.B.: Due to the intrinsic module logic, the minimum length of the Circular Buffer (corresponding to DESIRED LENGTH=0) is 2 CLOCK cycles. For all settings, 2 real CLOCK cycles occur in addition to the set value.
3.6. CONFIGURATION REGISTER PROGRAMMING

Via the Configuration Register (§ 4.7) it is possible to program the following:

- the BUSY signal enable on the “BUSY” connector;
- the "DIGOR OUT" configuration, i. e. the logic OR function of the inputs according to 4 pre-defined patterns, see § 4.7;
- the number N of 32-bit words to be transferred in the Multi-event Buffer upon receipt of a Trigger signal (N must lie between 3 and 15).

It is suggested not to use the value of 13 for the Number of transferred words. Moreover, the special value of 0 sets the module in TRANSPARENT mode, i. e. the input data are stored directly on the Multi-event Buffer for all the duration of the TRIGGER signal.

3.7. DATA ACQUISITION

As stated above, upon receipt of a Trigger signal, N 32-bit words and the relevant Event Number are stored respectively in the Multi-event Buffer and in the Event Number Register. The acquisition software can recognize this occurrence by reading continuously the STATUS word (Polling Mode, see § 4.2, § 4.4) until the EFEVCNT bit becomes = 1, or after an INTERRUPT occurrence.

Due to the internal structure of the Multi-event Buffer chips, the readout of the Data in memory must always be preceded by a test on the EFDATA bit in the STATUS word. If the EFDATA bit is 0 the first Datum is not valid; it is necessary to perform a dummy readout, after which it is possible to read the N valid Data in loop or via a VME access in Block Transfer Mode (D32 mode only).

3.8. CIRCULAR BUFFER TEST

In order to verify the correct functioning of the module, it is possible to write a known pattern in the circular Buffer and to use the software CLOCK and TRIGGER signals. The write operation must be preceded (just as in the case of the software CLOCK and TRIGGER operations) by a Disable Acquisition operation. After this it is necessary to do the following:

- write the desired pattern in the FIFO Writing Register (see § 4.11);
- perform a software CLOCK operation by writing in the CLOCK Register (see § 4.13).

The 32-bit word stored in the circular buffer will be constituted of 4 identical bytes reproducing the written pattern.
4. VME INTERFACE

4.1. ADDRESSING CAPABILITY

The V533 module works in A24 D16/D32 mode. This implies that the module's address must be specified in a field of 24 bits. The Address Modifiers codes recognized by the module are:

- AM=%3D: standard supervisor data access
- AM=%39: standard user data access
- AM=%0D: extended supervisor data access
- AM=%09: extended user data access

The module's Base Address is fixed by 2 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 4.1).

The Base Address can be selected in the range:

% 00 0000 <-> % FF 0000  A24 mode

The Base Address reserves in this way a page of 64 Kbytes for the module. The Address Map is shown in table 4.1.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>REGISTER/CONTENT</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base + %FFFF</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td></td>
<td>.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>.</td>
<td></td>
</tr>
<tr>
<td>Base + %1C</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>Base + %1A</td>
<td>TRIGGER</td>
<td>write only</td>
</tr>
<tr>
<td>Base + %18</td>
<td>CLOCK</td>
<td>write only</td>
</tr>
<tr>
<td>Base + %16</td>
<td>LOAD</td>
<td>read/write</td>
</tr>
<tr>
<td>Base + %14</td>
<td>FIFO Writing Register</td>
<td>write only</td>
</tr>
<tr>
<td>Base + %12</td>
<td>FIFO Low Readout</td>
<td>read only</td>
</tr>
<tr>
<td>Base + %10</td>
<td>FIFO High Readout</td>
<td>read only</td>
</tr>
<tr>
<td>Base + %0E</td>
<td>Enable/Disable Acquisition</td>
<td>write only</td>
</tr>
<tr>
<td>Base + %0C</td>
<td>Configuration Register</td>
<td>read/write</td>
</tr>
<tr>
<td>Base + %0A</td>
<td>RESET Register</td>
<td>write only</td>
</tr>
<tr>
<td>Base + %08</td>
<td>V2 Output Set</td>
<td>read/write</td>
</tr>
<tr>
<td>Base + %06</td>
<td>V1 Output Set</td>
<td>read/write</td>
</tr>
<tr>
<td>Base + %04</td>
<td>Event Number</td>
<td>read only</td>
</tr>
<tr>
<td>Base + %02</td>
<td>STATUS Register</td>
<td>read only</td>
</tr>
<tr>
<td>Base + %00</td>
<td>INTERRUPT Register</td>
<td>read/write</td>
</tr>
</tbody>
</table>
4.2. INTERRUPT LEVEL/VECTOR REGISTER
(Base Address + %00, read/write)

This register contains the value of the INTERRUPT Level and the STATUS/ID that the V533 INTERRUPTER places on the VME data bus during the INTERRUPT Acknowledge cycle. At Power-on or after a RESET this Register is cleared.

- Bits 0 to 5 are the 6 most significant bits of the INTERRUPT STATUS/ID; the two least significant bits of the STATUS/ID (not seen in the Register) are set to 0. This implies that the User should encode the INTERRUPT STATUS/ID as a multiple of 4, and store it in the INTERRUPT Register after dividing it by four.
- Bits 6 to 8 contain the INTERRUPT Level. The INTERRUPT generation can be disabled by writing 0 into these three bits.
- Bits 9 to 15 are not used.
4.3. STATUS REGISTER
(Base Address + %02, read only)

A read access to this Register returns the STATUS word, whose content is the following:

- Bit 0 is the Event Counter Memory Not Empty bit, set to 1 if the Event Counter Memory is Not Empty (EFEVCNT); this bit contains a don’t care value in case of TRANSPARENT mode functionality.
- Bit 1 is the Data Memory Not Empty bit, set to 1 if the Data Memory is Not Empty (EFDATA);
- Bit 2 is the Data Memory Almost Full bit, set to 0 if the Data Memory is Almost Full (7 words to become Full; PAF);
- Bit 3 is the Module Busy bit, set to 1 if the Module is BUSY:
- Bits 4 through 15 are not used.

At Power-on or after a RESET the PAF bit is set to 1 while the EFDATA and EFEVCNT are set to 0.

The occurrence of PAF=0 causes a STOP in the acquisition, a disabling of the external signals and a generation of the BUSY signal (if enabled) on the “BUSY” connector.
4.4. EVENT NUMBER REGISTER
(Base Address + %04, read only)

A 16-bit read access to this Register returns on the 8 MSBs the Event Number, and on the 8 LSBS the STATUS word, see § 4.3.

As the memories are FIFOs, the Event Number readout must be performed together with the Data readout, in order to maintain the correct association between the two informations.

The Event Number associated to the first trigger occurred after Power-On or a RESET is 0.

![Figure 4.4: Event Number Register](image)

4.5. V1/V2 OUTPUT SET REGISTERS
(Base Address + %06, + %08, read/write)

A read (write) access to these Registers allows the readout (writing) of the output values V1 and V2. These are Voltage levels programmable on 8 bits between +5 V (value 0) and -5 V (value 255):

- a value of 0 in the address Base + %06 produces an output of +5 V on the V1 output; a value of 255 produces an output of -5 V on the V1 output.
- a value of 0 in the address Base + %08 produces an output of +5 V on the V2 output; a value of 255 produces an output of -5 V on the V2 output.

![Figure 4.5: V1/V2 Output Set Registers](image)
4.6. **RESET REGISTER**  
(Base Address + %0A, write only)

A 16-bit write access to this address causes a global RESET of the module. This operation must be preceded by a Disabling of the external signals, see § 4.8.

In order to be effective on the two memory buffers, the RESET must be followed by a CLOCK command, see § 4.13.

4.7. **CONFIGURATION REGISTER**  
(Base Address + %0C, read/write)

A read (write) access to this Register enables the readout (writing) of the Configuration Register, whose content is the following:

- Bits 0 to 3 contain the number of 32-bit words to be transferred from the pipeline memory to the multi-event buffer. Minimum value is 3, maximum value is 15, it is suggested not to use a value of 13. The special value 0 sets the module in TRANSPARENT Mode.

- Bits 4 to 6 set the OR configuration of the module, according to the following:
  - 000 selects the first configuration, in which, on the 16 couples of pins in the "DIGOR OUR" connectors, are available the ORs of the couples of adjacent channels (CH0#CH1, CH2#CH3, ..., CH30#CH31);
  - 001 selects the second configuration, in which, on the 8 couples of pins in the rightmost "DIGOR OUR" connector, are available the ORs of the quadruples of adjacent channels (CH0#CH1#CH2#CH3, ..., CH28#CH29#CH30#CH31);
  - 010 selects the third configuration, in which, on the 4 top couples of pins in the rightmost "DIGOR OUR" connector, are available the ORs of the octuples of adjacent channels (CH0#CH1#...#CH7, ..., CH24#CH25#...#CH31);
  - 011 selects the fourth configuration, in which, on the 2 top couples of pins in the rightmost "DIGOR OUR" connector, are available the ORs of the groups of 16 adjacent channels (CH0#CH1#...#CH16, CH17#CH18#...#CH31);
  - 1xx is not used.

- Bit 7 set to 1 allows the BUSY signal generation on the "BUSY" connector.

- Bits 8 to 15 are not used.

The content of the Configuration Register is not defined at Power-On and is not affected by a RESET operation.
4.8. **ENABLE/DISABLE ACQUISITION**  
(Base Address + %0E, write only)

A 16-bit write access to this Register with the DB8 bit of the Data Bus set to 0 enables the external signals (Inputs, CLK and TRIG).

A 16-bit write access to this Register with the DB8 bit of the Data Bus set to 1 disables the external signals (Inputs, CLK and TRIG).

4.9. **FIFO HIGH READOUT**  
(Base Address + %10, read only)

A 16-bit read access to this Register enables the readout of the 16 MSBs of the Multi-event Buffer Data Word.

A 32-bit read access to this Register enables the readout of the complete Multi-event Buffer Data Word.

4.10. **FIFO LOW READOUT**  
(Base Address + %12, read only)

A 16-bit read access to this Register enables the readout of the 16 LSBs of the Multi-event Buffer Data Word.

4.11. **FIFO WRITING REGISTER**  
(Base Address + %14, write only)

In order to program the FIFO buffer length, the User must perform the series of operations described above (see § 3.5). The value LENGTH to be written in the bits DB0-DB7 of the Data Bus is:

\[ \text{LENGTH} = 255 - \text{DESIRED LENGTH}, \]

i. e., if the User wants to use a FIFO length of 100, he/she has to program a value of 155 in the 8 LSBs of the FIFO Writing Register.

This Register can also be used for test purposes, see § 3.8.
4.12. LOAD REGISTER  
(Base Address + %16, read/write)

A 16-bit write access to this address sets the LOAD internal line to 0, a 16-bit read access to this address sets the LOAD internal line to 1.

4.13. CLOCK REGISTER  
(Base Address + %18, write only)

A 16-bit write access to this address generates an internal CLOCK pulse. This operation must be preceded by a Disabling of the external signals, see § 4.8.

4.14. TRIGGER REGISTER  
(Base Address + %1A, write only)

A 16-bit write access to this address generates an internal TRIGGER pulse. This operation must be preceded by a Disabling of the external signals, see § 4.8.